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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,977	10/28/2003	Kia Silverbrook	ZG001US	9653

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SILVERBROOK RESEARCH PTY LTD
393 DARLING STREET
BALMAIN, 2041
AUSTRALIA

EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,977	SILVERBROOK, KIA	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/112,767.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/112,767, filed on July 10, 1998.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Drive circuitry, a plurality of ink inlet channels and nozzle arrangements, a passive nozzle chamber structure, a dynamic nozzle chamber structure, and an elongate micro-electromechanical actuator are critical or essential to the practice of the invention, but not included in the claim, are not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Applicant's claim 1 requires the inkjet printhead include the features of drive circuitry, a plurality of ink inlet channels and nozzle arrangements, a passive nozzle chamber structure, a dynamic nozzle chamber structure, and an elongate micro-electromechanical actuator, however the active process steps do not include a method for forming these features.

4. Claims 2-6 are rejected under 35 U.S.C. 112, first paragraph, because they are dependent on a non-enabled base claim.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

6. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

7. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-6 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 of U.S. Patent No. 6,502,306,

Silverbrook ("Silverbrook I"), in view of Choi et al. (U.S Patent No. 5,909,230) and Silverbrook (U.S. Patent No. 6,180,427) ("Silverbrook II").

9. As to claim 1, Silverbrook I claims a method, comprising the steps of: depositing a first layer of a sacrificial material on the wafer substrate (claim 1, column 8, lines 45-46); forming a deposition zone for the passive beam and the passive structure with the first layer of sacrificial material (claim 1, column 8, line 47); depositing a metal layer on the first layer of sacrificial material (claim 1, column 8, line 48-49); etching the metal layer to define the passive beam and the passive structure (claim 1, column 8, line 51); depositing a second layer of a sacrificial material on the metal layer (claim 1, column 8, line 52-53); forming a deposition zone for the active beam on the second layer of sacrificial material (claim 1, column 8, line 54); depositing a metal layer on the second layer of sacrificial material (claim 1, column 8, lines 55-56); etching the metal layer to define the active beam (claim 1, column 8, line 57), the deposition zone being formed so that the metal layer makes electrical contact with the drive circuitry (claim 3, column 9, lines 4-8); depositing a third layer of sacrificial material on the metal layer (claim 3, column 9, lines 58-59); forming a deposition zone for the dynamic structure on the third layer of sacrificial material (claim 1, column 8, line 61); depositing a structural layer on the third layer of sacrificial material (claim 1, column 8, line 62-63); etching the structural layer to define the dynamic structure; and etching away the sacrificial material (claim 1, column 8, lines 65-67). It should be noted that Silverbrook I's claim 1 is directed at a MEMS device that is positioned on a wafer substrate that incorporates drive circuitry (claim 1, column 8, lines 41-43). However, Silverbrook II teaches that a MEMS device

on a wafer substrate with drive circuitry is commonly used to form inkjet printheads because fabrication relies on standard circuit construction and fabrication techniques of depositing planar layers on silicon (column 7, lines 12-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a method of fabricating a MEMS device on a wafer substrate with drive circuitry to form an inkjet printhead. One who is skilled in the art would be motivated use a common fabrication method, known to accomplish the task of forming an inkjet printhead. Moreover, one who is skilled in the art would be motivated to adopt Silverbrook II's method, because it is know to accomplish the task of forming an inkjet printhead.

10. Silverbrook I does not expressly claim an inkjet printhead chip, as claimed by the Applicant. However, Choi discloses a method of fabricating an inkjet printhead chip for an inkjet printhead (column 1, lines 6-14), the inkjet printhead chip having a wafer substrate (100) (column 3, lines 48-49; Figure 5) that incorporates drive circuitry (column 4, lines 56-65) and defines a plurality of ink inlet channels and nozzle arrangements (column 3, lines 66-67; column 4, lines 1-2; Figure 5) that each have a passive nozzle chamber structure that extends from the wafer substrate and bounds a respective ink inlet channel (120/112) (Figure 8; column 4, lines 12-19), a dynamic nozzle chamber structure (111) that, together with the passive structure (120), defines a nozzle chamber (120/111), and has a roof that defines the ink ejection port (column 4, lines 12-19), the dynamic structure (111) being displaceable towards the wafer substrate into an actuated position and away from the wafer substrate into a rest position (Figures 9A-9B) such that a drop of ink (101) can be ejected from the ink

ejection port (112) (column 5, lines 42-61), and an elongate micro-electromechanical actuator connected between the wafer substrate and the dynamic structure, the actuator including a beam assembly that has an active beam of a conductive material (300), capable of thermal expansion (column 5, lines 6-11), that defines a heating circuit and is connected to the drive circuitry and a passive beam that is interposed between the active beam and the wafer substrate such that, when the active beam receives an electrical signal from the drive circuitry, the active beam expands relative to the passive beam driving the dynamic structure into the actuated position to generate the drop of ink and when the signal is cut off subsequent cooling of the active beam causes the dynamic structure to move back to the rest position, facilitating a separation of the drop of ink (column 4, lines 1-2; column 5, lines 1-11; Figures 5 and 9A-9B). Choi's inkjet chip includes the advantages of achieving maximum resolution by minimizing distances between adjacent ink ejection ports, prevent the blocking of ejection ports by reducing their length, creating a more reliable device (column 2, lines 34-42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Silverbrook I's method to form Choi's inkjet chip. One who is skilled in the art would be motivated to form an inkjet chip with higher resolution and reliability.

11. As to claim 2, Silverbrook II discloses that the steps of depositing the metal layers each comprise the step of depositing titanium nitride (column 12, lines 58-62).

12. As to claim 3, Silverbrook II discloses that the step of forming a deposition zone for the dynamic structure includes the step of forming a deposition zone for an arm that

interconnects the dynamic structure and the beam assembly (column 12, lines 65-67; Figure 23).

13. As to claim 4, Silverbrook II discloses that the step of depositing the structural layer includes the step of depositing a layer of a dielectric material that is adhesive to metal, such that the structural layer adheres to the passive and active beams (column 12, lines 63-67; Figure 23).

14. As to claim 5, Silverbrook II does not expressly disclose that the step of depositing the first layer of sacrificial material includes the step of depositing the first layer of sacrificial material to a depth of between five and twelve microns. However, for other sacrificial layers, Silverbrook II teaches thicknesses between 1 and 10 microns (column 11, lines 11-13, lines 30-31). It should be noted that there is overlap between Applicant's thickness range and Silverbrook II's range. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select a sacrificial material to a depth of between five and twelve microns. One who is skilled in the art would be motivated to select a thickness range similar to Silverbrook II's method, which is know to accomplish the task of forming an inkjet printhead chip.

15. As to claim 6, Silverbrook II discloses the step of applying a release tape (column 13, line 4) to the structural layer to permit retention of the printhead chip in a suitable position and etching the inlet channels through the wafer substrate and into each nozzle chamber (column 13, lines 12-19), prior to etching away the sacrificial material (column 13, lines 20-22; Figure 28).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC
June 29, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER